REMARKS

Applicants respectfully request that the Amendment and Response to Final Office Action be admitted under 37 C.F.R. 1.116. Applicants submit that this amendment presents claims in better form for consideration on appeal. Furthermore, applicants believe that consideration of this amendment could lead to favorable action that would remove one or more issues for appeal. Applicants submit that, thus, there is good and sufficient reason why this amendment should be admitted now. Reconsideration of this application, as amended, is respectfully requested. Claims 1-15 are pending. Claims 1-15 stand rejected. Claims 6-10 have been objected to.

Claims 1, 6, and 11 have been amended. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Claim Objections

Claim 6 has been amended to address the objection.

Rejections Under 35 U.S.C. § 103(a)

Claims 6-8, 10-13 and 15 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,480,948 of Virajpet, et al. ("Virajpet"), U.S. Patent No. 6,240,519 of James, Jr., et al. ("James"), and U.S. Patent No. 6,262,594 of Cheung, et al. ("Cheung").

The Examiner has rejected claims 6-8, 10-13 and 15 under 35 U.S.C. § 103 as being unpatentable over Virajpet, James, and Cheung. The Examiner has stated that

> Regarding claims 6 and 11, Virajpet, et al. teaches a system for memory aliasing system. The processor is able to read from an internal ROM (31) for initialization (configuration) or boot code processing (col. 3, lines 1-16; col. 4, lines 5-23). Section (31) of the memory map is configurable, and during a first time period, the configurable section is aliased so that when the processor attempts to access this section (internal ROM), the access is directed toward the external ROM (20) under control of the bus/memory controller. Thus, when the processor seeks to address 00000000h, the access is directed toward an external non-volatile memory.

A first difference between the claimed subject matter and that of Virajpet, et al., disclosed supra, is that the claim recites searching for a valid secondary initialization routine. James, Jr., et al. teaches a system for recovering from a corrupted boot ROM image. The ROM image found within the ROM device, and once the processor determines that the image is corrupt, the processor continues to execute the boot block code of the ROM (col. 7, lines 54-58; col. 8, lines 4-12; Fig. 6A-6D). James, Jr., et al. teaches searching for a secondary init. Routine in the form of determining if a floppy disk (external memory) is present in the floppy drive. If the diskette is present, the boot sequence is initialized from the floppy disk without the aid of the original ROM (col. 8, line 53 – col. 9, line 1). Booting of the original ROM was disabled in order for the diskette boot sequence to occur.

Another difference between the claimed subject matter and that of Virajpet, et al. and James, Jr., et al. is that the claims recite that the aliasing is done for a configurable system-on-chip system. Cheung, et al. teaches a configurable system-on-chip design. According to Figure 4, which illustrates specific modules that may be incorporated onto a system-on-chip configuration, Cheung, et al. teaches an external memory system coupled to the system-on-a-chip in the form of an external flash ROM (non-volatile memory) (col. 7, lines 56-60). Also, an erasable read-only-memory is taught for storing control values (col. 3, lines 14-16), where the ROM is found on the system-on-chip. Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Virajpet, et al., James, Jr., et al., and Cheung, et al. before him at the time the invention was made to modify the aliasing system of Virajpet, et al. to include the recoverable ROM system of James, Jr., et al. and the system-on-chip design of Cheung, et al., because then a single integrated circuit chip would yield advantages of cost reduction, low power consumption, space savings and ruggedness, as taught by Cheung, et al., as well as teach a system for reflashing a corrupted ROM for future use, as taught by James, Jr., et al.

Regarding claims 7 and 12, Virajpet, et al. teaches loading initialization operations from an external non-volatile memory (flash) (col. 4, lines 9-13).

Regarding claims 8 and 13, the changing of aliases as taught by Virajpet, et al. is done during a first time period following processor reset, such that the processor must re-initialize from the external memory (col. 3, lines 8-13).

Regarding claims 10 and 15, Virajpet, et al. teaches a continuing program for the initialization program setup. As seen in Figure 3, should the select signal be set, the internal ROM is directed to return requested date (col. 5, lines 12-16).

(p. 3-5, Office Action 7/9/03)

Claims 1-3 and 5 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,480,948 of Virajpet, et al. ("Virajpet"), U.S. Patent No. 6,240,519 of James, Jr., et al. ("James"), and U.S. Patent No. 6,262,594 of Cheung, et al. ("Cheung").

The Examiner has rejected claims 1-3 and 5 under 35 U.S.C. § 103 as being unpatentable over Virajpet, James, and Cheung. The Examiner has stated that

> Regarding claim 1, Virajpet, et al. teaches a system for memory aliasing system. The processor is able to read from an internal ROM (31) for initialization (configuration) or boot code processing (col. 3, lines 1-16; col. 4, lines 5-23). Section (31) of the memory map is configurable, and during a first time period, the configurable section is aliased so that when the processor attempts to access this section (internal ROM), the access is directed toward the external ROM (20) under control of the bus/memory controller. Thus, when the processor seeks to address 00000000h, the access is directed toward an external non-volatile memory.
>
> A first difference between the claimed subject matter and that of Virajpet, et al., disclosed supra, is that the claim recites searching for a valid secondary initialization routine. James, Jr., et al. teaches a system for recovering from a corrupted boot ROM image. The ROM image found within the ROM device, and once the processor determines that the image is corrupt, the processor continues to execute the boot block code of the ROM (col. 7, lines 54-58; col. 8, lines 4-12; Fig. 6A-6D). James, Jr., et al. teaches searching for a secondary init. Routine in the form of determining if a floppy disk (external memory) is present in the floppy drive. If the diskette is present, the boot sequence is initialized from the floppy disk without the aid of the original ROM (col. 8, line 53 – col. 9, line 1). Booting of the original ROM was disabled in order for the diskette boot sequence to occur.
>
> Another difference between the claimed subject matter and that of Virajpet, et al. and James, Jr., et al. is that the claims recite that the aliasing is done for a configurable system-on-chip system, as well as that the external memory is a flash memory. Cheung, et al. teaches a configurable system-on-chip design. According to Figure 4, which illustrates specific modules that may be incorporated onto a system-on-chip configuration, Cheung, et al. teaches an external flash ROM (non-volatile memory) with a flash ROM interface (col. 7, lines 56-60). Also, an erasable read-only-memory is taught for storing control values (col. 3, lines 14-16), where the ROM is found on the system-on-chip. One of ordinary skill in the art would recognize that he routines stored on the floppy diskette external memory of Jones, Jr., et al. could just as easily by stored and implemented in a secondary ROM device like that of Cheung, et al. The system of James, et al. uses floppy disk to store the boot initialization routine and flashing code in fact (col. 9, lines 8-12). Implementation of the secondary ROM device would negate the increased financial cost, as well as the increased system size, of a floppy disk drive. The Examiner takes Official Notice of these teachings. Therefore it would have been obvious

to one of ordinary skill in the art having the teachings of Virajpet, et al., James, Jr., et al., and Cheung, et al. before him at the time the invention was made to modify the aliasing system of Virajpet, et al. to include the recoverable ROM system of James, Jr., et al. and the system-on-chip design of Cheung, et al., because then a single integrated circuit chip would yield advantages of cost reduction, low power consumption, space savings, and ruggedness, as taught by Cheung, et al., as well as teach a system for reflashing a corrupted ROM for future use, as taught by James, Jr., et al.

Regarding claim 2, Virajpet, et al. teaches loading initialization operations from an external non-volatile memory (flash) (col. 4, lines 9-13).

Regarding claim 3, the changing of aliases as taught by Virajpet, et al. is done during a first time period following processor reset, such that the processor must re-initialize from the external memory (col. 3, lines 8-13).

(p. 5-7, Office Action 7/9/03)

Applicants respectfully submit, however, that amended claim 1 is not obvious under 35 U.S.C. § 103 in view of Virajpet, James, and Cheung. Amended claim 1 includes the following limitations.

A method for multiple memory aliasing for a configurable system-on-a-chip, the configurable system on a chip integrating at least a central processing unit, an internal system bus, and a programmable logic, on a single integrated circuit device, the method comprising:

executing code from a read-only memory (ROM) internal memory, said ROM internal memory having an alias;

searching for a valid secondary initialization routine;

locating a configuration program in the ROM internal memory;

disabling the ROM internal memory alias; and

jumping to the secondary initialization routine located in a FLASH external memory.

(Amended claim 1) (Emphasis added)

Applicants respectfully contend that the system on a chip of Cheung does not claim to be configurable and cannot be equated to the claimed "configurable system-on-a-chip." In Cheung, the use of the pads is configurable, allowing a sharing of pads. In contrast, a configurable system-on-a-chip ("CSOC"), as claimed, integrates at least a CPU, an internal system bus, and programmable logic.

It is also respectfully submitted that Virajpet and Cheung do not teach or suggest a combination with James and that James does not teach or suggest a combination with Virajpet and Cheung. It would be impermissible hindsight based on applicants' own disclosure to incorporate the configurable memory map of Virajpet and the method for configuring groups of pads of a system on a chip of Cheung with the method for governing flashing of a new ROM image as disclosed in James. Moreover, such a combination would still lack the limitations of amended claim 1 as discussed above.

For these reasons, applicants respectfully submit that amended claim 1 is not rendered obvious by Virajpet in view of James and Cheung.

Given that claims 2, 3, and 5 depend, directly or indirectly, from claim 1, applicants submit that claims 2, 3, and 5 are, likewise, not obvious under § 103 in view of the combination of Virajpet, James and Cheung. Moreover, given that amended claims 6 and 11 contain the limitation of a configurable system-on-a-chip, applicants respectfully submit that amended claims 6 and 11, and through dependency thereon, claims 7, 8, 10 and claims 12, 13, and 15, respectively, are likewise, not obvious under § 103 in view of the combination of Virajpet, James and Cheung.

Claims 4, 9 and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,480,948 of Virajpet, et al. ("Virajpet"), U.S. Patent No. 6,240,519 of James, Jr., et al., ("James"), U.S. Patent No. 6,262,594 of Cheung, et al. ("Cheung"), and U.S. Patent No. 6,401,164 of Bartoli, et al. ("Bartoli").

Applicants respectfully submit, however, that claims 4, 9, and 14 are not obvious under 35 U.S.C. § 103 in view of Virajpet, James, Cheung and Bartoli due to their dependence upon claims 1, 6, and 11, respectively, as discussed above.

It is also respectfully submitted that none of Virajpet, James, and Cheung teach or suggest a combination with Bartoli, nor does Bartoli teach or suggest a combination with Virajpet, James, and Cheung. It would be impermissible hindsight based on applicants' own disclosure to incorporate the configurable memory map of Virajpet, the method for configuring groups of pads of a system on a chip of Cheung, and the method for governing flashing of a new ROM image of James, with the memory device of Bartoli. Moreover, such a combination would still lack the claimed limitations as discussed above.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 11/07/03 By: _____
Tom Van Zandt
Reg. No. 43,219

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8598